



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Nick A. Youker et al. Examiner: Nitin Parekh  
Serial No.: 09/970,145 Group Art Unit: 2811  
Filed: October 2, 2001 Docket: 279.361US1  
Title: METHOD AND SYSTEM OF TAPE AUTOMATED BONDING

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents  
MS: Appeal Brief-Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Applicant respectfully requests review of the final rejection provided in the Final Office Action dated September 13, 2005 and maintained in the Advisory Action dated February 9, 2006. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

Regarding the §102 Rejection of claims 7-9, 11, 12 and 20-25 as being anticipated by Buckley, III, et al. (U.S. Patent No. 5,477,082).

Claims 7-9 and 20-22

Applicant maintains the position in the response mailed January 13, 2006 that claims 7-9, and 20-22 are not anticipated by the cited reference since the cited reference does not include each and every element of the claimed invention, arranged as in the claim.

Applicant believes there is a clear error of fact in the Examiner's position since each limitation recited in claim 1 is not found in the cited reference. For instance, Buckley does not include an electrical component mounted on or above a surface of the IC chip and electrically connected to the IC chip via "a lead on the TAB leadframe which extends outward from the electrical component to a perimeter I/O of the IC chip." In contrast, Buckley discusses a double-sided structure where the devices 56, 58A, 90 are connected to each other and contacts 24A of a leadframe through vias 22. (See Figs. 3 and 6 of Buckley).

In the Response to Arguments section of the Office Action mailed September 13, 2005, the Examiner states that Buckley discloses component 94 being mounted above/below a surface of the IC chip and electrically connected "to the IC chip via respective lead pads/leads, which

extend outward ... from the second IC chip/electrical component to the perimeter bonding pads/I/O pads IC chip." However, this subject matter is not disclosed in the Buckley reference. In contrast, in Buckley the only connection between the two IC chips (e.g. 56, 90 in Fig. 6) is through via vertically oriented holes 22. There is no indication that the leads connected to chip 90 extend *outward* from chip 90 to a perimeter I/O of chip 56. Accordingly, the cited reference does not include a lead on the TAB leadframe which extends outward from the electrical component to a perimeter I/O of the IC chip, as recited in claim 7.

Claims 8, 9, and 20-22 include each limitation of their parent claim and are therefore also not anticipated by the cited reference. Reconsideration and allowance is respectfully requested.

Claims 11, 12, and 23-25

Applicant maintains the position in the response mailed January 13, 2006 that claims 11, 12 and 23-25 are not anticipated by the cited reference since the cited reference does not include each and every element of the claimed invention, arranged as in the claim.

Applicant believes there is a clear error of fact in the Examiner's position since each limitation recited in claim 1 is not found in the cited reference. In this case, Applicant cannot find in the cited reference: wherein at least one of the plurality of leads is internally routed relative to the ILB area so that the at least one lead has a contact exposed interior to the ILB portion of the TAB structure and above a major surface of the IC chip; and an electrical component mounted on or above the major surface of the IC chip and electrically connected to the IC chip via the at least one lead which has a contact exposed interior to the ILB portion of the TAB structure and above a major surface of the IC chip.

Again, Buckley discusses a double-sided structure where the devices 56, 58A, and 90 are connected to each other and contacts 24A of a leadframe through vias 22. (See Figs. 3 and 6 of Buckley). The leads are not internally routed as asserted by the Examiner; they are merely vertical vias, as discussed above. Accordingly, the cited reference does not include at least one lead internally routed relative to the ILB area so that the at least one lead has a contact exposed interior to the ILB portion of the TAB structure and above a major surface of the IC chip, as recited in claim 11.

Claims 12 and 23-25 include each limitation of their parent claim and are therefore also

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not anticipated by the cited reference. Reconsideration and allowance is respectfully requested.

*Regarding the §103 Rejection of claims 10 and 13 as being unpatentable over Buckley, III, et al.*  
*(U.S. Patent No. 5,477,082) in view of admitted prior art (APA).*

Claims 10 and 13 include each limitation of their parent claims and are not obvious in view of the cited references for the reasons given above. Reconsideration and allowance is respectfully requested.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 359-3267 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

NICK A. YOUKER ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
P.O. Box 2938  
Minneapolis, MN 55402  
(612) 359-3267

Date 3/13/06 By Peter C Maki  
Peter C Maki  
Reg. No. 42,832

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, MS/Appeal Brief-Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 13 day of March, 2006.

Name Peter C Maki

Signature Peter C Maki